What is claimed is:

1. A vertical double channel silicon-on-insulator (SOI) field-effect-transistor (FET), comprising:

a pair of two vertical semiconductor layers in contact with a pair of parallel shallow trench isolation layers on a substrate;

a source, a drain and a channel region on each of the pair of vertical semiconductor layers with corresponding regions on the pair of vertical semiconductor layers facing each other in alignment;

a gate oxide on the channel region of both of the pair of the vertical semiconductor layers; and

a gate electrode, a source electrode, and a drain electrode electrically connecting the respective regions of the pair of vertical semiconductor layers.

2. The vertical double channel silicon-on-insulator (SOI) field-effect-transistor (FET) as claimed in claim 1, further comprising:

a bottom channel, having a higher threshold voltage than a threshold voltage of the channel region on each of the pair of vertical semiconductor layers, formed on the substrate.

3. The vertical double channel silicon-on-insulator (SOI) field-effect-transistor (FET) as claimed in claim 1, further comprising:

an insulator layer on top of the pair of parallel shallow trench isolation layers, on top of the substrate in between the pair of two vertical semiconductor layers, and in between middle portions of the pair of two vertical semiconductor layers on both sides of the gate electrode.

4. The vertical double channel silicon-on-insulator (SOI) field-effect-transistor (FET) as claimed in claim 1, wherein the FET is of planar type.

5. The vertical double channel silicon-on-insulator (SOI) field-effect-transistor (FET) as claimed in claim 1, wherein the gate electrode is formed of either tungsten silicide or tungsten.

6. A vertical double channel silicon-on-insulator (SOI) field-effect-transistor (FET) as claimed in claim 1, wherein the source/drain electrode is formed of either doped polysilicon or tungsten.

7. The vertical double channel silicon on insulator (SOI) field effect transistor (FET) as claimed in claim 1, wherein a depth of the pair of two vertical semiconductor layers is approximately 2/3 of a depth of the pair of parallel shallow trench isolation layers.

8. A vertical double channel silicon on insulator (SOI) field effect transistor (FET), comprising:

a. a substrate having an active region;

b. a pair of vertical shallow trench isolation (STI) regions in the active region of the substrate and extending in a longitudinal direction;

c. a pair of vertical source/drain regions adjacent to the pair of vertical shallow trench isolation regions with a transistor channel region between the source/drain regions in the active region of the substrate and extending in the longitudinal direction;

d. a bottom channel, having a higher threshold voltage than a threshold voltage of the transistor channel, formed on the substrate and in contact with both of the pair of vertical source/drain regions;

e. a first oxide layer formed on and above the pair of vertical shallow trench isolation regions;

f. a source/drain electrode formed within the first oxide layer, the source/drain electrode being formed on the pair of vertical source/drain regions;

g. a gate oxide layer formed between the pair of vertical source/drain regions on the bottom channel, the gate oxide layer formed in a lateral direction at a midsection of the substrate; and

h. a gate electrode formed on the pair of shallow trench isolation regions and the gate oxide layer.

9. The vertical double channel silicon on insulator (SOI) field effect transistor (FET) as claimed in claim 8, further comprising:

a gate mask formed on the gate electrode.

10. The vertical double channel silicon on insulator (SOI) field effect transistor (FET) as claimed in claim 8, further comprising:

a second oxide layer formed on the bottom channel and between the pair of vertical source/drain regions adjacent to the gate electrode.

11. The vertical double channel silicon on insulator (SOI) field effect transistor (FET) as claimed in claim 8, further comprising:

a sidewall spacer formed on an upper surface of the vertical source/drain regions.

12. The vertical double channel silicon on insulator (SOI) field effect transistor (FET) as claimed in claim 8, wherein the gate mask is a silicon nitride layer.

13. The vertical double channel silicon on insulator (SOI) field effect transistor (FET) as claimed in claim 8, wherein the pair of vertical shallow trench isolation regions have a depth of about 3000 Å.

14. The vertical double channel silicon on insulator (SOI) field effect transistor (FET) as claimed in claim 8, wherein the vertical source/drain regions have a depth of about 2000 Å.

15. A method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET), comprising:

a. forming a pair of shallow trench isolation (STI) regions in an active region of a substrate so that an upper surface of the shallow trench isolation regions protrudes above an upper surface of the substrate;

b. performing a first ion implantation process on the active region of the substrate to form a pair of vertical transistor channels and a bottom channel, wherein the pair of vertical transistor channels and the bottom channel extend in a longitudinal direction;

c. forming sidewall spacers on the active region of the substrate above the pair of vertical transistor channels and adjacent to the protruding portion of the pair of shallow trench isolation regions;

d. etching the active region of the substrate, using the sidewall spacers as a mask, to expose the pair of vertical transistor channels and the bottom channel, wherein the pair of vertical transistor channels and the bottom channel define a trench;

e. performing a second ion implantation process on the exposed bottom channel;

f. forming a gate oxide layer between the pair of vertical transistor channels on the bottom channel in a lateral direction at a midsection of the substrate;

g. forming a gate electrode on the gate oxide layer, the sidewall spacers, and an upper surface of the pair of vertical shallow trench isolation regions;

h performing a third ion implantation process on the exposed pair of vertical transistor channels to form a pair of vertical source/drain regions;

i depositing an oxide layer on the bottom channel, the sidewall spacers, and an upper surface of the shallow trench isolation regions so that the oxide layer is adjacent to the gate oxide layer and the gate electrode, the oxide layer filling the trench;

j etching the oxide layer to expose an upper portion of the pair of vertical source/drain regions; and

k forming a source/drain contact electrode on the bottom channel and between the pair of vertical source/drain regions so that an upper surface of the source/drain contact electrode is even with an upper surface of the gate mask.

16. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 15, further comprising:

forming a gate mask on the gate electrode after forming the gate electrode .

17. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 15, wherein forming the pair of STI regions comprises:

a. depositing a mask layer on the substrate;

b. performing an anisotropic etching process to remove the mask layer and form a pair of trench regions; and

c. filling the pair of trench regions with an insulating layer.

18. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 17, wherein the mask layer is a silicon nitride layer.

19. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 17, wherein the etching process to remove the mask layer is a wet etching.

20. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 15, wherein the

first ion implantation process is a low dose implantation performed at an implant angle of 0°.

21. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 15, wherein the second ion implantation process is a high dose implantation performed at an angle of 0°.

22. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 15, wherein the third ion implantation process is performed at a tilted implant angle.

23. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 22, wherein the tilted implant angle is 7°.

24. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 15, wherein the third ion implantation process is a plasma doping process.

25. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 15, wherein forming the sidewall spacer comprises:

a. depositing a spacer layer on an upper surface of the substrate including the protruding portion of the shallow trench isolation region; and

b. etching the spacer layer using an anisotropic etching method to form the sidewall spacers adjacent to the protruding portion of the shallow trench isolation region.

26. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 25, wherein the spacer layer is formed by either a low-pressure chemical vapor deposition (LPCVD) silicon nitride or a plasma-enhanced chemical vapor deposition (PECVD) silicon nitride.

27. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 26, wherein the spacer layer is deposited to a thickness of between about 500 Å to 800 Å.

28. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 15, wherein the sidewall spacers have a thickness of about 500 Å.

29. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 15, wherein the gate oxide layer is a thermally grown oxide.

30. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 16, wherein forming the gate electrode and forming the gate mask comprises:

depositing the gate electrode on the gate oxide layer, the sidewall spacers, and an upper surface of the pair of vertical shallow trench isolation regions using a low-pressure chemical vapor deposition (LPCVD) process;

planarizing the gate electrode layer using a chemical mechanical polishing (CMP);

depositing the gate mask on the planarized gate electrode layer using a LPCVD process; and

patterning the gate mask and the gate electrode using photolithography and etching.

31. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 15, wherein the gate electrode is formed of either tungsten silicide or tungsten.

32. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 16, wherein the gate mask is a silicon nitride layer.

33. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 15, wherein the source/drain contact electrode is formed of either doped polysilicon or tungsten.

34. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 15, wherein the trench is etched using a reactive ion etching (RIE).

35. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 15, wherein the trench is etched to a depth of about 2000 Å.

36. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 15, wherein the shallow trench isolation regions have a depth of about 3000 Å.

37. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 15, wherein the

bottom channel has a high threshold voltage of equal to or greater than about 2 V.

38. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 15, wherein an etching depth of the trench is approximately 2/3 of a depth of the shallow trench isolation region.

39. A method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET), comprising:

a. forming a pair of shallow trench isolation (STI) regions in an active region of a substrate so that an upper portion of the shallow trench isolation regions protrudes above an upper surface of the substrate;

b. forming sidewall spacers on the active region of the substrate adjacent to the protruding portion of the pair of shallow trench isolation regions;

c. etching the active region of the substrate, using the sidewall spacers as a mask, to define a trench;

d. performing a first ion implantation process on sidewalls and a bottom portion of the trench to form a pair of vertical transistor channels and a bottom channel, respectively, wherein the pair of vertical transistor channels and the bottom channel extend in a longitudinal direction;

e. forming a gate oxide layer between the pair of vertical transistor channels on the bottom channel in a lateral direction at a midsection of the substrate;

f. forming a gate electrode on the gate oxide layer, the sidewall spacers, and an upper surface of the pair of vertical shallow trench isolation regions;

g. performing a second ion implantation process on the exposed pair of vertical transistor channels to form a pair of vertical source/drain regions;

h. depositing an oxide layer on the bottom channel, the sidewall spacers, and an upper surface of the shallow trench isolation regions, wherein the oxide layer is adjacent to the gate oxide layer and the gate electrode, the oxide layer filling the trench;

i. etching the oxide layer to expose an upper portion of the pair of vertical source/drain regions; and

j. forming a source/drain contact electrode on the bottom channel and between the pair of vertical source/drain regions so that an upper surface of the source/drain contact electrode is even with an upper surface of the gate mask.

40. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 39, further comprising:

forming a gate mask on the gate electrode after forming the gate electrode.

41. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 39, wherein forming the STI regions comprises:

a. depositing a mask layer on the substrate;

b. performing an anisotropic etching process to remove the mask layer and form a pair of trench regions; and

c. filling the pair of trench regions with an insulating layer.

42. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 41, wherein the mask layer is a silicon nitride layer.

43. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 41, wherein the etching process to remove the mask layer is a wet etching.

44. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field-effect-transistor (FET) as claimed in claim 39, wherein the first ion implantation process comprises:

a tilted low dose ion implantation process to form the pair of vertical transistor channels; and

a zero angle high dose ion implantation process to form the bottom channel.

45. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field-effect-transistor (FET) as claimed in claim 39, wherein the first ion implantation process comprises a plasma doping process.

46. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 39, wherein the second ion implantation process is performed at a tilted implant angle.

47. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 46, wherein the tilted implant angle is 7°.

48. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 39, wherein the second ion implantation process is a plasma doping process.

49. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 39, wherein forming the sidewall spacer comprises:

a. depositing a spacer layer on an upper surface of the substrate including the protruding portion of the shallow trench isolation region; and

b. etching the spacer layer using an anisotropic etching method to form the sidewall spacers adjacent to the protruding portion of the shallow trench isolation region.

50. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 49, wherein the spacer layer is formed by either a low-pressure chemical vapor deposition (LPCVD) silicon nitride or a plasma-enhanced chemical vapor deposition (PECVD) silicon nitride.

51. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 50, wherein the spacer layer is deposited to a thickness of between about 500 Å to 800 Å.

52. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 39, wherein the sidewall spacers have a thickness of about 500 Å.

53. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 39, wherein the gate oxide layer is a thermally grown oxide.

54. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 40, wherein forming the gate electrode and forming the gate mask comprises:

depositing the gate electrode on the gate oxide layer, the sidewall spacers, and an upper surface of the pair of vertical shallow trench isolation regions using a low-pressure chemical vapor deposition (LPCVD) process;

planarizing the gate electrode layer using a chemical mechanical polishing (CMP);

depositing the gate mask on the planarized gate electrode layer using a LPCVD process; and

patterning the gate mask and the gate electrode using photolithography and etching.

55. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 39, wherein the gate electrode is formed of either tungsten silicide or tungsten.

56. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 40, wherein the gate mask is a silicon nitride layer.

57. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 39, wherein the source/drain contact electrode is formed of either doped polysilicon or tungsten.

58. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 39, wherein the trench is etched using a reactive ion etching (RIE).

59. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 39, wherein the trench is etched to a depth of about 2000 Å.

60. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 39, wherein the shallow trench isolation regions have a depth of about 3000 Å.

61. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 39, wherein the

bottom channel has a high threshold voltage of equal to or greater than about 2 V.

62. The method of manufacturing a vertical double channel silicon-on-insulator (SOI) field effect transistor (FET) as claimed in claim 39, wherein an etching depth of the trench is approximately 2/3 of a depth of the shallow trench isolation region.